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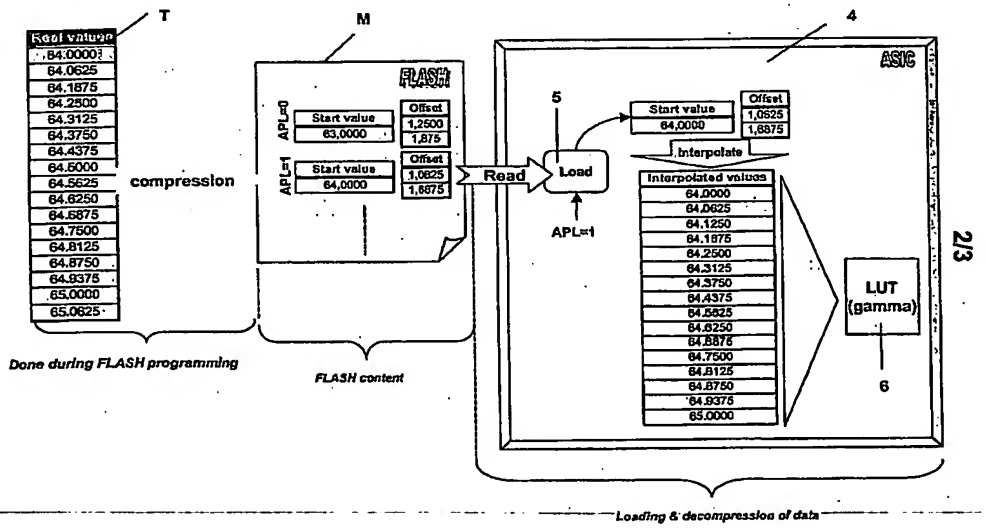
(54) Title: METHOD AND APPARATUS FOR INTERPOLATING DATA IN THE VIDEO PICTURE FIELD



(57) Abstract: The present invention relates to a method for interpolating N data from n values (n < N and N/n = p, p being an integer), the n values corresponding to points on a curve which can be linearly approximated, said method comprising the following steps: a) calculating n offset values such as: $Offset_k = data_{(k+1)*p} - data_{k*p}$ with k = 0, 1, 2, ...n, b) storing the n offset values and a start value in a memory, c) interpolating the N data, by calculating: $data_{p*k+a} = data_{p*k} + a*offset_k/p$ where a varies between 1 and p. The invention is mainly applicable to plasma display panel.

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METHOD AND APPARATUS FOR INTERPOLATING DATA IN THE VIDEO PICTURE FIELD

The present invention relates to a method for interpolating data in the video picture field. It also relates to a circuit for implementing said method.

The present invention is particularly useful in the field of plasma display panels (PDPs) or other display devices wherein each video level is represented by a combination of bits according to a specific coding. In this case, when the algorithms used to improve picture quality are based on data stored in memories such as look-up tables (LUTs), the size of such tables may be quite huge.

BACKGROUND OF THE INVENTION

To understand the problem, the present invention will be described in relation with PDP but may be applicable to other types of display or other apparatus processing video display and requiring memories with huge size.

To improve picture quality in PDPs, a lot of algorithms has been developed, using data stored in look-up tables. For example, in EP patent application No. 02 290 907.1 published under No. 1353314, is described a method for improving grey scale fidelity portrayal based on a modification of the coding approach for each power level (APL) that occurs at each frame. More specifically, for a given peak white level, the sustain pulses are distributed among the sub-fields, the number of pulses corresponding to the sub-field weighting. Then, the sub-field codes are mapped to luminance codes, which are re-ordered in a definite order. Moreover, the video levels are mapped to the available luminance codes and processed to achieve intermediate levels of luminance. Then, the luminance codes are mapped to the output sub-field codes. In this case, look-up tables (LUTs) are used at least for mapping the video levels to the luminance codes and for mapping

the luminance codes to the output sub-field codes. These look-up tables, which contain, for example, luminance codes to be loaded for each new APL level are stored in an external memory. These tables are quite huge. For instance, the size of a standard look-up table is calculated for handling numbers of 12 bits with 8 bits for the integral part of the number plus 4 bits for the factional part. The input and output from the LUT are on 12 bits. So, all look-up tables used for and after gamma have a size of 4096 x 12 bits = 49152 bits.

In the case of 8-bit average power level, at least 256 look-up tables (LUTs) are necessary, requesting 256 x 49152 = 12582912 bits (12Mbit) in the external memory. Moreover, each LUTs could be different for the three colors, which increases the total amount of memory required to 36Mbit. In the case of the concept described above called Metacode concept, it is necessary to update this LUT for each frame. Soat least 36Mbit are necessary in the external memory only for the Metacode concept with high bandwidth requirements since only a part of the vertical blanking is available to reload the table. Furthermore, these LUTs are also different for each mode used in the PDP (e.g. 60Hz, 50Hz, 75Hz...), which further increases the needs in terms of external memory since 3 modes equal 3 x 36 Mbit = 108 Mbit.

It is the purpose of the present invention to propose a way to compress and uncompress the data to solve previously presented issues.

SUMMARY OF THE INVENTION

So, the invention proposes a method for interpolating N data from n values (n < N and $\frac{N}{n} = p$, p being an integer), the n values corresponding to points on a curve which can be linearly approximated, said method comprising the following steps :

a) calculating n offset values such as :

$offset_k = data_{(k+1)*p} - data_{k*p}$

with k = 0, 1, 2, ...n,

b) storing the n offset values and a start value in a memory,

c) interpolating the N data, using an interpolation function.

Such function is a linear function and the N data is obtained by calculating :

$$data_{p*k+a} = data_{p*k} + \frac{a * offset_k}{p}$$

where a varies between 1 and p.

Other interpolation functions may be used such as a spine function or a quadratic function based on three samples .

According to a preferred embodiment, the start value is an integer.

This method is particularly useful when the data stored in the memory are ordered in an ascending manner. This is the case when the data corresponds to gamma or to data coded using a code such as the gravity center code GCC as described in EP 01 250 158.1. However, one bit for sign may be added to the data (the offset values) stored in the memory. So, it is possible to have a mix of ascendant and descendant values.

In fact, the main idea is to store only a part of the values to be interpolated inside a controller made as an ASIC (Application Specific Integrated Circuit).

In addition, the storage of the values is done in a way to reduce the amount of stored data and the bandwidth requirements.

The present invention relates also to a circuit for implementing the above method mainly comprising an external memory including first look-up tables storing offset values and start values corresponding to specific values and a controller including an average picture power measurement circuit sending a specific value to a memory interface dedicated to read the offset value and the start value stored in a look-up table of the external memory corresponding to said specific value and an interpolation interface to

interpolate data from the offset value and the start value and send the interpolated data to a second internal look-up table.

DRAWINGS

Exemplary embodiments of the invention are illustrated in the drawings and are explained in more detail in the following description with reference to said drawings, wherein:

Figure 1 is a schematic explaining the method of the present invention.

Figure 2 is an example of memory programming and decompression step.

Figure 3 is a schematic of a possible implementation of the invention.

DESCRIPTION OF PREFERRED EMBODIMENTS

The present invention will be described with reference to a coding using average power level or APL values. As shown in figure 1, in the external memory part M, for each APL sample 1 (APL = 0 .....APL = 256 in the present example), the degamma function follows a curve as represented by 2.

According to the method of the present invention, only some values according to points 3 of the curve 2 are stored in the LUTs of the external memory M in a compressed manner, as explained below. After each refresh of the ASIC block 4, the offset values and the start value corresponding to the required APL level are loaded in the circuit load 5. Then, the values for the whole LUT are obtained with the interpolation function 7 implementing the method of the present invention.

So, for each APL, the values (offset values and start value) of a new sampled LUT will be loaded and then, the interpolation will occur inside the ASIC to obtain the final and complete LUT.

In order to better understand the principle, a practical example will be described. This example corresponds to the generation, storage, compression and decompression of a 12 bits x 12 bits LUT (4096 positions,

each one with 12 bits). In that case, as an example, the 12 bits data represent 8-bit integral value with 4 bit fractional.

For instance, the data really stored in the external memory contains 256 positions, each one based on 8 bits data representing the offset value to previous data and not the real value. More specifically, the offset values stored in the LUT of the external memory are obtained as follows:

$Offset_k = data_{(k+1)*p} - data_{k*p}$

With k = 0, 1, 2.... n

Then, at the beginning of the interpolation process, the starting value data-start for the LUT is loaded under the form of an 8 bit integer value. This value is an integer value without fractional part. So, when the interpolation function is a linear interpolation, the new sequence of data may be defined as following:

$data_{pk+a} = data_{pk} + \frac{a \times offset_k}{p}$ where $data_a$ represents the 12-bit data at position *m* to be stored in the real LUT on-chip inside the ASIC, *a* represents one of the p interpolated new values, (so, from 256 positions inside the external memory, 4096 have to be recreated), and $offset_k$ represents the offset to the next value used for interpolation stored in the external memory. In this concept, $data_0 = data\_start.*16$ (no fractional part) or $data\_start \ll 4$

A detailed example is shown below and represented in Figure 2.

Based on the real values given in the left table T, the external memory M that is, for example, a flash memory or an EPROM, stores for each APL (APL = 0, APL = 1, ... APL = 256) a start value that is an integer and 256 offset values determined by calculating the difference between two data regularly spaced on the curve. For example, for APL = 1 the start value equals 64.0000 and the first offset is equal to the 15th real value 65.0625 (see table T) – the start value 64.0000, so the offset equals to 1.0625. The second offset 1.6857 is obtained by subtracting the 31st data or

real value to the 16th real value and so on up to the 256th offset value. The same is done for the other APL, as shown for APL = 0 that starts with a start value equals to 63.000 and offset values equal to 1.2500, 1.875, ... in memory M.

Then, in the ASIC 4, the values stored in the memory M are read and loaded in relation with the APL value that is APL = 1 In the embodiment. The interpolation is done using the formula given in the method. In this case, p = 16 and the 16 interpolated values based on the sampled information start value = 64.0000 and first offset value = 1.0625 are calculated as follows:

Computation	Interpolated values
64 + (0 x 1.0625)/16	64.0000
64 + (1 x 1.0625)/16	64.0625
64 + (2 x 1.0625)/16	64.1250
64 + (3 x 1.0625)/16	64.1875
64 + (4 x 1.0625)/16	64.2500
64 + (5 x 1.0625)/16	64.3125
64 + (6 x 1.0625)/16	64.3750
64 + (7 x 1.0625)/16	64.4375
64 + (8 x 1.0625)/16	64.5625
64 + (9 x 1.0625)/16	64.6250
64 + (10 x 1.0625)/16	64.6875
64 + (11 x 1.0625)/16	64.7500
64 + (12 x 1.0625)/16	64.8125
64 + (13 x 1.0625)/16	64.8750
64 + (14 x 1.0625)/16	64.9375
64 + (15 x 1.0625)/16	65.0000

For the following 16 interpolated values, the offset value used for the interpolation is the second offset value, i.e. 1.6875 and so on for the 256 offset values.

This concept enables to have only 256 positions recorded inside the external LUT while disposing of a huge number of interpolated positions inside the ASIC. In the example, only 16 positions are computed from the

data extracted of the FLASH memory M giving the possibility to obtain 4096 positions from the 256 values stored. However, it is possible to extract much more position by simply changing the value 16 in the next formula:

$$data_{16k+a} = data_{16k} + \frac{a \times offset_k}{16}.$$

The main advantages of the concept presented here leads in a strong reduction of size of the external memory required by the PDP ASIC 4 to store all LUTs, i.e. one LUT per APL value, per color and per mode for a specific application such as gamma, GCC, Metacode. This reduction is also very important for the bandwidth limitation of the interface external memory/ASIC, which enables to load much more data in the same time frame, i.e. vertical blanking.

For instance, in the computation done in the introduction, 108Mbit for 3 modes are needed whereas, with the concept of the invention, only 256 x 8 x 256 x 3 x 3 = 4.5 Mbit are needed.

A possible implementation of the method of the invention is shown in figure 3.

In the embodiment, the plasma display controller 10 includes the usual circuits (not shown) such as the video degamma circuit, the sub-field coding circuit, the serial-parallel conversion circuit and the controller per se. So it is possible to include all these circuits in a same ASIC. From the controller 10 are sent the scan and the sustain signals to the drivers of a plasma display panel 11.

The look-up table data is stored on an external memory 12 (EPROM or FLASH) that can be read bit sequentially by the controller 10. In normal operation at the end of every frame, new LUT data has to be downloaded by the controller depending on the APL value that has been computed during the active part of the video based on R, G and B information by the APL measurement circuit 10a. Each refresh operation of the LUTs is based on three blocks: the memory interface 10b that simply reads at a specific address inside the memory 12 a certain amount of bits,

an interpolation interface 10c dedicated to each LUTs of the ASIC in order to perform the appropriate data interpolation and finally a loading block 10d in charge of loading the specific LUTs with their respective interpolated data.

The main idea is to transfer all the look-up tables data from the external memory 12 inside the on-chip memory in the ASIC 10 using pins SCLK and SDATA, at the end of each frame during the vertical blanking. Indeed, it takes a complete active frame to compute the APL level required to load the right LUTs and it is not allowed to change the content of any LUT during the displaying of active part, otherwise the pictures will lose their homogeneity.

Once the new APL level has been determined, the controller 10 will request the required data from the external memory 12, and will load the required table data inside the whole ASIC, as explained above.

The here presented solution reduces memory and bandwidth costs for all LUTs related to PDP signal processing such as gamma, GCC, metacode. The added logic on the memory controller has negligible impact on the die area. Moreover, the number of addresses required inside the external memory is lower than what is required by the final LUT size (interpolation factor) so that the memory interface can be simplified too.

According to another feature of the invention, if the signal processing required mix of ascendant and descendant values, a bit for sign is added to the data (the offset values) stored in the external memory.

In the above embodiment a linear interpolation function has been described. However, other type of interpolation functions may be used as mentioned in the introductory part.

The invention is described with reference to a PDP display but it is obvious that the invention is applicable to other displays or apparatus having to store a huge amount of data.

CLAIMS

1 – Method for interpolating N data from n values (n < N and $\frac{N}{n} = p$, p being an integer), the n values corresponding to points on a curve which can be linearly approximated, said method comprising the following steps:

a) calculating n offset values such as:

$offset_k = data_{(k+1)*p} - data_{k*p}$

with k = 0, 1, 2, ...n,

b) storing the n offset values and a start value in a memory,

d) interpolating the N data using an interpolation function.

2 – Method according to claim 1 characterized in that the interpolation function is a linear function, a spine function or a quadratic function based on several samples.

3 – Method according to claim 2 characterized in that the N data of the linear function are obatined by calculating:

$$data_{p*k+a} = data_{p*k} + \frac{a * offset_k}{p}$$

where a varies between 1 and p.

4 – Method according to any of claims 1 to 3, characterized in that the data are ordered in an ascending manner.

5 – Method according to any of claims 1 to 3, characterized in that a bit for sign is added to the offset values for a mix of ascendant and descendant order.

6 – Method according to any of claims 1 to 5, characterized in that the start value is an integer.

7 – Circuit for implementing the method according to any of claims 1 to 6, characterized in that it comprises an external memory including first look-up tables for storing offset values and start values corresponding to specific values and a controller including a measuring circuit sending a specific value to a memory interface dedicated to read the offset value and the start value stored in a look-up table of the external memory corresponding to said specific value and an interpolation interface to interpolate data from the offset value and the start value and send the interpolated data to a second look-up table.

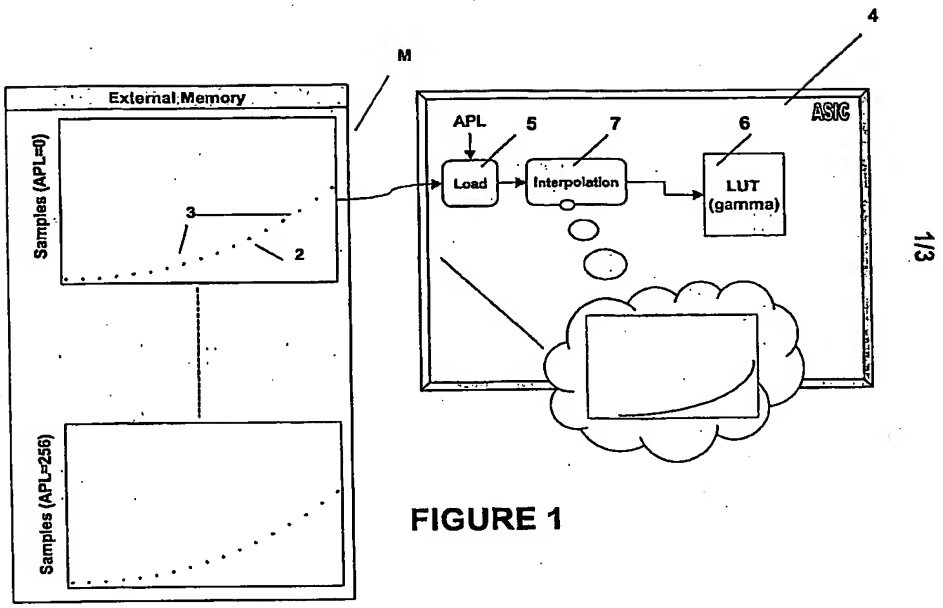

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FIGURE 1

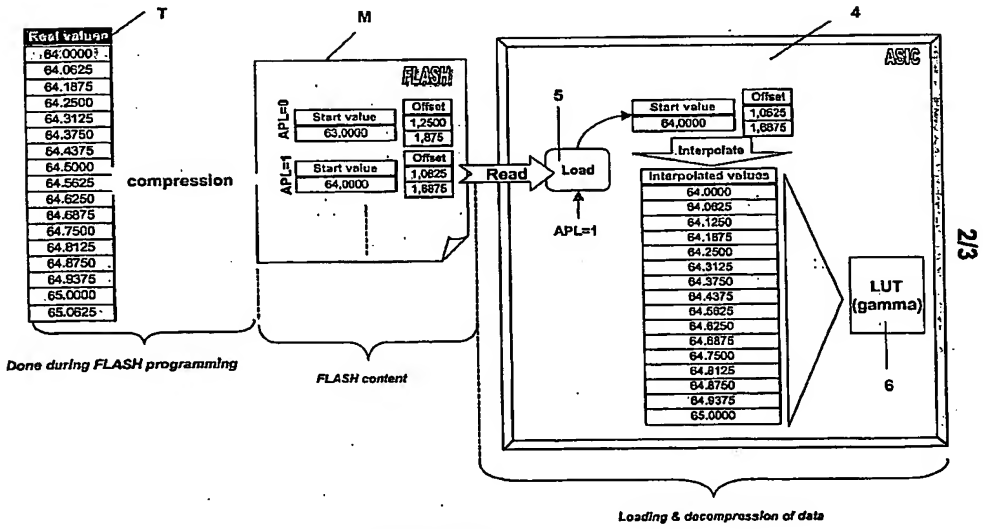

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FIGURE 2

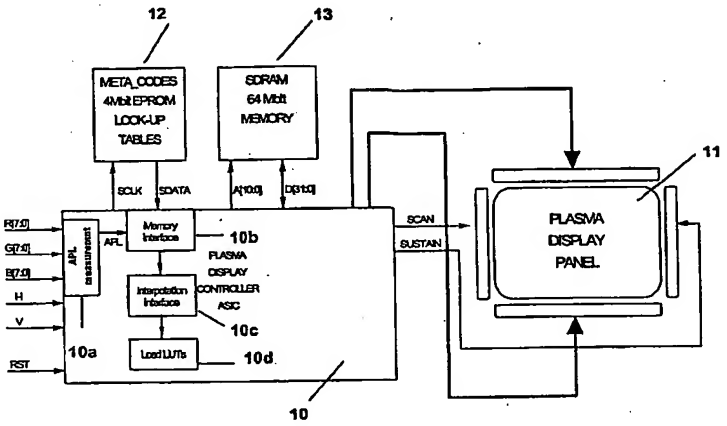
12
13
META_CODES
4Mbit EPROM
LOOK-UP
TABLES
SDRAM
64 Mbit
MEMORY
SCLK
SDATA
A[10:0]
D[31:0]
R[7:0]
G[7:0]
B[7:0]
H
V
RST
APL measurement
APL
Memory Interface
10b
PLASMA DISPLAY CONTROLLER ASIC
Interpolation Interface
10c
Load LUTs
10d
10a
10
SCAN
SUSTAIN
PLASMA
DISPLAY
PANEL
11

FIGURE 3

INTERNATIONAL SEARCH REPORT

International Application No
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A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H04N9/69

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H04N G09G G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, PAJ, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2002/030690 A1 (YOSHII HIDEKI ET AL) 14 March 2002 (2002-03-14) Image processing method for image display apparatus, involves varying spacing between interpolation points according to high spatial frequency information. abstract paragraph '0003! - paragraph '0008!; figures 1-5 paragraph '0009! - paragraph '0017! paragraph '0152! - paragraph '0160!; figure 19 paragraphs '0088!,'0095! -/--	1-7

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"A" document defining the general state of the art which is not considered to be of particular relevance

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
13 September 2004	11/10/2004

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax (+31-70) 340-3016	Wolff, L

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INTERNATIONAL SEARCH REPORT

International Application No
PCT/EP2004/050837

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 137 542 A (VAN MOURIK JOHANNES G R) 24 October 2000 (2000-10-24)	1,3-6
Y	Combination of a linear approximation and a look up table in order to increase the resolution of a gamma correction for PDP (Plasma display panel) abstract the whole document column 2, line 8 -column 3, line 14; figure 4	2,7
Y	US 6 002 810 A (SATO HIROKO ET AL) 14 December 1999 (1999-12-14) abstract Resolution conversion apparatus in accordance with conversion magnification factor: interpolation includes linear, spline functions and Bezier functions	2,7
A	PATENT ABSTRACTS OF JAPAN vol. 017, no. 588 (P-1634), 27 October 1993 (1993-10-27) -& JP 05 173523 A (HITACHI LTD), 13 July 1993 (1993-07-13) Data converters which consist of LUTs and which adjust data of each data converter by using arithmetic interpolation processing : Pictures evenness and uniformity can be obtained. abstract	1-7
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INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/EP2004/050837

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